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Objective:

An opportunity to utilize my skills in physical, circuit, and logic design through a position in engineering or research beginning in October 1998.

Experience:

11/96-present **Adaptec, Inc.**, Peripheral Technology Solutions Division, Longmont, CO
Research and Development Engineer

- Designed part of a buffer controller block to be used in a hard disk drive controller (HDC) chip. The block was designed to be fully synchronous so that scan could be inserted with the help of Synopsys. The logic design was done in Verilog-XL, the synthesis was done in Synopsys, and static timing was done in Primetime.
- Designed part of a fully synchronous error detection and correction (EDAC) block to be used in a HDC chip. Responsibilities included the buffer block interface, CRC syndrome update machine, and correction FIFO circuitry.
- Designed clock trees for several different HDC chips operating at a maximum frequency of 100 MHz. Each chip had two distinct clock domains, one of which had components of 100 MHz and 50 MHz. There were free-running and gated clocks (for conservation of power) with widely varying loads. The skew between clocks had to be managed to within 0.5ns across all process corners. In addition to the circuit design, I directed the physical design of the clock tree networks and I automated the back-annotation of capacitance into the SPICE netlists to simplify the task of circuit verification.
- Wrote assembly language tests to fault grade a buffer controller block within an HDC chip. The chip did not have scan so all manufacturing test vectors had to be written by hand and then simulated with Verifault to discover the test coverage. I had the opportunity to add some test registers to the block before fabrication, which eased the task. I also directed two co-op students in writing tests for this effort.
- Acted as liaison between the physical design group and the logic design group.

5/95-11/96 **Hewlett-Packard Company**, Integrated Circuits Business Division, Ft. Collins, CO
Research and Development Engineer

- Optimized register file and math interface unit for a geometry accelerator ASIC. The final circuit used the same CMOS process as the original, but was 53% smaller and operated at 165 MHz for a 22% speedup. Responsibilities included schematic design, full-custom physical layout, and functional and timing verification of the circuit.
- Designed, synthesized, and verified an IEEE 1149.1 Test Access Port (TAP) controller for a graphics ASIC. Added special functions for testing math megacells, examining internal state, and implementing an IDDQ test in addition to the IEEE 1149.1 standard functionality. The TAP was defined using Verilog and synthesized with Synopsys.
- Optimized layout and verified timing of control blocks (approximately 20,000 gates each) by running place and route tool, back-annotating capacitances back into Synopsys, and resynthesizing (using compile in place) in an iterative loop. All tools used were HP internal tools except for Synopsys.
- Created chip model and generated scan tests with the Sunrise tool.
- Extracted and simulated clock skew at the chip level using SPICE.
- Automated design tasks with Korn Shell and Perl scripts.

8/94-5/95 **Optoelectronic Computing Systems Center**, University of Colorado, Boulder, CO
Research Assistant

- Designed and simulated pixel arrays for spatial light modulators (SLMs). The SLMs were designed in a standard CMOS IC process with additional steps to add the liquid crystal material. Responsibilities included circuit design, SPICE simulation, and physical design.

- Researched novel graphics architectures and displays including three-dimensional (3-D) displays. This research culminated in a design for a time-multiplexed autostereoscopic 3-D display that was ideal for the SLMs that we were producing. A **C** program that generated images for the display was also written.
- Conducted tutorials on the lift-off process used for fabrication of the SLMs.

5/94- **Cyrix Corporation**, System Technology Lab, Longmont, CO
8/94 Summer Intern
- Wrote technical summaries for patent applications. Patents covered a clock generator for a memory controller and architectures for advanced x86 compatible microprocessor designs.

8/93- **Electrical and Computer Engineering Department**, University of Colorado, Boulder, CO
5/94 Teaching Assistant
- Taught microprocessor lab which emphasized assembly language programming, C, and the 8088 microprocessor.
- Conducted recitation and lab sections for basic circuit theory.

1/93- **Rockwell International**, Collins Avionics Division, Cedar Rapids, IA
7/93 Cooperative Education Student, Integrated Circuits Design
- Designed pixel array and driver circuitry for advanced active matrix liquid crystal display (AMLCD) in a silicon-on-insulator (SOI) process. Responsibilities included schematic design, determining timing requirements with the use of SPICE, and producing the physical layout for the entire chip.
- Performed physical layout for GaAs analog chip designs.

5/92- **Rockwell International**, Collins Avionics Division, Cedar Rapids, IA
8/92 Cooperative Education Student, FCS Autopilot Design
- Modified main microprocessor system in FCC-4000 autopilot to operate at 10 MHz instead of 6 MHz. The autopilot was a dual microprocessor system that used Intel and Motorola processors. The hardware and software on the associated test equipment was also redesigned. The software was written in C and 6805 assembly language.
- Performed detailed economic analysis to find least expensive way to retrofit old FCC-4000's with the speed upgrade.

5/91- **Rockwell International**, Collins Avionics Division, Cedar Rapids, IA
8/91 Cooperative Education Student, Computer Hardware Design
- Diagnosed problem on FCC-702 power supply monitor and modified the monitor.
- Modified software and hardware on ITS automatic test station.

8/90- **Rockwell International**, Collins Avionics Division, Cedar Rapids, IA
12/90 Cooperative Education Student, Aircraft Systems Integration
- Wrote Turbo Pascal code to enhance flight simulation programs.
- Wrote a reference manual for flight simulation program and made additions to the Integration Lab User's Guide.

1/90- **Rockwell International**, Collins Avionics Division, Cedar Rapids, IA
5/90 Cooperative Education Student, Reliability
- Performed reliability tests on Rockwell equipment including radar systems and auto-pilots.
- Tracked performance of Rockwell equipment in the field.

Education:
- M.S. Electrical Engineering, May 1996, University of Colorado, Boulder, CO, GPA: 3.83/A=4.0.
- B.S. Electrical Engineering, December 1992, University of Wyoming, Laramie, WY, GPA: 3.86/A=4.0.
- Electrical Engineering Student of the Year (1992).
- Professionally registered Engineering in Training (EIT).

References:
Available upon request.